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APPLICATION NO.	FILING DATE	FIRST NAMED INVENTOR	ATTORNEY DOCKET NO.	CONFIRMATION NO.
10/644,156	08/20/2003	Shi-Dong Zhou	X-1477 US	5800

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EXAMINER	
COX, CASSANDRA F	

ART UNIT	PAPER NUMBER
2816	

DATE MAILED: 08/25/2004

Please find below and/or attached an Office communication concerning this application or proceeding.

Office Action Summary	Application No.	Applicant(s)	
	10/644,156	ZHOU ET AL.	
	Examiner	Art Unit	
	Cassandra Cox	2816	

-- The MAILING DATE of this communication appears on the cover sheet with the correspondence address --

Period for Reply

A SHORTENED STATUTORY PERIOD FOR REPLY IS SET TO EXPIRE 3 MONTH(S) FROM THE MAILING DATE OF THIS COMMUNICATION.

- Extensions of time may be available under the provisions of 37 CFR 1.136(a). In no event, however, may a reply be timely filed after SIX (6) MONTHS from the mailing date of this communication.
- If the period for reply specified above is less than thirty (30) days, a reply within the statutory minimum of thirty (30) days will be considered timely.
- If NO period for reply is specified above, the maximum statutory period will apply and will expire SIX (6) MONTHS from the mailing date of this communication.
- Failure to reply within the set or extended period for reply will, by statute, cause the application to become ABANDONED (35 U.S.C. § 133). Any reply received by the Office later than three months after the mailing date of this communication, even if timely filed, may reduce any earned patent term adjustment. See 37 CFR 1.704(b).

Status

1)☒ Responsive to communication(s) filed on *20 August 2003*.

2a)☐ This action is **FINAL**. 2b)☒ This action is non-final.

3)☐ Since this application is in condition for allowance except for formal matters, prosecution as to the merits is closed in accordance with the practice under *Ex parte Quayle*, 1935 C.D. 11, 453 O.G. 213.

Disposition of Claims

4)☒ Claim(s) *1-30* is/are pending in the application.

4a) Of the above claim(s) _____ is/are withdrawn from consideration.

5)☒ Claim(s) *14-22* is/are allowed.

6)☒ Claim(s) *1-2, 10, 13, 23-24, 28-29* is/are rejected.

7)☒ Claim(s) *3-9,11,12,25-27 and 30* is/are objected to.

8)☐ Claim(s) _____ are subject to restriction and/or election requirement.

Application Papers

9)☐ The specification is objected to by the Examiner.

10)☒ The drawing(s) filed on *20 August 2003* is/are: a)☒ accepted or b)☐ objected to by the Examiner.

Applicant may not request that any objection to the drawing(s) be held in abeyance. See 37 CFR 1.85(a).

Replacement drawing sheet(s) including the correction is required if the drawing(s) is objected to. See 37 CFR 1.121(d).

11)☐ The oath or declaration is objected to by the Examiner. Note the attached Office Action or form PTO-152.

Priority under 35 U.S.C. § 119

12)☐ Acknowledgment is made of a claim for foreign priority under 35 U.S.C. § 119(a)-(d) or (f).

a)☐ All b)☐ Some * c)☐ None of:

1.☐ Certified copies of the priority documents have been received.

2.☐ Certified copies of the priority documents have been received in Application No. _____.

3.☐ Copies of the certified copies of the priority documents have been received in this National Stage application from the International Bureau (PCT Rule 17.2(a)).

* See the attached detailed Office action for a list of the certified copies not received.

Attachment(s)

1) ☒ Notice of References Cited (PTO-892)
2) ☐ Notice of Draftsperson's Patent Drawing Review (PTO-948)
3) ☒ Information Disclosure Statement(s) (PTO-1449 or PTO/SB/08) Paper No(s)/Mail Date *08/20/03*.
4) ☐ Interview Summary (PTO-413) Paper No(s)/Mail Date. _____ .
5) ☐ Notice of Informal Patent Application (PTO-152)
6) ☐ Other: _____.

DETAILED ACTION

Claim Rejections - 35 USC § 112

1. The following is a quotation of the second paragraph of 35 U.S.C. 112:

> The specification shall conclude with one or more claims particularly pointing out and distinctly claiming the subject matter which the applicant regards as his invention.

2. Claim 10 is rejected under 35 U.S.C. 112, second paragraph, as being indefinite for failing to particularly point out and distinctly claim the subject matter which applicant regards as the invention.

3. Claim 10 recites the limitation "shunt transistors" in line 2 of the claim. There is insufficient antecedent basis for this limitation in the claim.

Claim Rejections - 35 USC § 102

4. The following is a quotation of the appropriate paragraphs of 35 U.S.C. 102 that form the basis for the rejections under this section made in this Office action:

> A person shall be entitled to a patent unless –
>
> (e) the invention was described in (1) an application for patent, published under section 122(b), by another filed in the United States before the invention by the applicant for patent or (2) a patent granted on an application for patent by another filed in the United States before the invention by the applicant for patent, except that an international application filed under the treaty defined in section 351(a) shall have the effects for purposes of this subsection of an application filed in the United States only if the international application designated the United States and was published under Article 21(2) of such treaty in the English language.

5. Claims 1-2, 13, 23-24, and 28-29 are rejected under 35 U.S.C. 102(e) as being anticipated by Chiu et al. (U.S. Patent No. 6,472,912).

In reference to claim 1, Chiu discloses in Figure 2 a power-on reset circuit (200) to generate a reset signal (Vx), comprising: a pull-up resistor (R3) connected between a supply voltage (VDD) and a tracking node; a pull-down transistor (M1) connected between the tracking node and ground potential, the tracking node generating a voltage

(Vx) indicative of the reset signal; and a voltage divider circuit (Z1, Z2) connected between the supply voltage (VDD) and ground potential, the voltage divider circuit (Z1, Z2) having a first ratioed voltage node (210) coupled to the gate of the pull-down transistor (M1). The same applies to claims 23-24 (wherein the voltage divider is seen to be the same as the means for generating the control voltage) and 28.

In reference to claim 2, Chiu discloses in column 1, lines 34-35 that the voltage divider circuit (Z1, Z2) comprises: a first resistor (Z1) connected between the voltage supply (VDD) and the first ratioed voltage node (210); and a second resistor (Z2) connected between the first ratioed voltage node (210) and ground potential.

In reference to claim 13, Chiu does not say that the power-on reset circuit (200) is part of a programmable logic device, however it is considered well-known to one skilled in the art that power-on reset circuits can be used as part of a programmable logic device, of which fact official notice is taken.

In reference to claim 29, Chiu discloses in Figure 2 that the control voltage (Vi) is a predetermined fraction of the supply voltage.

Allowable Subject Matter

6. Claims 14-22 are allowed.

7. Claims 3-9, 11-12, 25-27, and 30 are objected to as being dependent upon a rejected base claim, but would be allowable if rewritten in independent form including all of the limitations of the base claim and any intervening claims.

8. The following is a statement of reasons for the indication of allowable subject matter: Claims 3-9 would be allowable because the closest prior art of record fails to disclose a circuit as shown in Figure 2 wherein the voltage divider circuit comprises a third resistor (R3) and a shunt transistor (MN2) connected between the second ratioed voltage node (V2) and ground potential, and having a gate responsive to the reset signal in combination with the rest of the limitations of the base claims and any intervening claims. Claims 11-12 would be allowable because the closest prior art of record fails to disclose a circuit as shown in Figure 2 wherein the circuit further comprises a buffer circuit (230) in combination with the rest of the limitations of the base claims and any intervening claims. Claims 25-27 and 30 would be allowable because the closest prior art of record fails to disclose a circuit as shown in Figure 2 wherein the circuit further comprises means (MN2) for selectively adjusting the predetermined factor in response to the reset signal (RST) in combination with the rest of the limitations of the base claims and any intervening claims.

9. The following is an examiner's statement of reasons for allowance: Claims 14-22 are allowed because the closest prior art of record fails to disclose a circuit as shown in Figure 2 wherein the circuit comprises a third resistor (R3) and a second transistor (MN2) connected between the second ratioed voltage node (V2) and ground potential, and having a gate responsive to the reset signal in combination with the rest of the limitations of the base claims and any intervening claims.

Any comments considered necessary by applicant must be submitted no later than the payment of the issue fee and, to avoid processing delays, should preferably

accompany the issue fee. Such submissions should be clearly labeled "Comments on Statement of Reasons for Allowance."

Conclusion

10. The prior art made of record and not relied upon is considered pertinent to applicant's disclosure.

Any inquiry concerning this communication or earlier communications from the examiner should be directed to Cassandra Cox whose telephone number is 571-272-1741. The examiner can normally be reached on Monday-Thursday from 8:00 AM to 5:30 PM and on.

If attempts to reach the examiner by telephone are unsuccessful, the examiner's supervisor, Timothy Callahan can be reached on 571-272-1740. The fax phone number for the organization where this application or proceeding is assigned is 703-872-9306.

Information regarding the status of an application may be obtained from the Patent Application Information Retrieval (PAIR) system. Status information for published applications may be obtained from either Private PAIR or Public PAIR. Status information for unpublished applications is available through Private PAIR only. For more information about the PAIR system, see http://pair-direct.uspto.gov. Should you have questions on access to the Private PAIR system, contact the Electronic Business Center (EBC) at 866-217-9197 (toll-free).

CC
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August 17, 2004

TIMOTHY P. CALLAHAN
SUPERVISORY PATENT EXAMINER
TECHNOLOGY CENTER 2800